What is claimed is:

~~1. A display panel including a first~~ substrate having an array region and an array peripheral region, and a second substrate having a black matrix, the display panel comprising:

a plurality of gate lines on the first substrate;

a gate insulating film on the first substrate including the gate lines;

a plurality of data lines arranged to cross the gate lines, for defining a pixel region on the array region; and

a light leakage prevention film formed between the gate lines and/or data lines of the array peripheral region, for preventing light leakage.

~~2. The display panel further comprising:~~

a TFT and a pixel electrode formed in each pixel region.

3. The display panel as claimed in claim 2, further comprising:

the second substrate having the black matrix and a color filter layer and facing the first substrate; and

a liquid crystal layer formed between the first and second substrates.

4. The display panel as claimed in claim 1, wherein the light leakage prevention film is formed simultaneously with at least one of the gate lines.

5. The display panel as claimed in claim 4, wherein the light leakage prevention film is formed to prevent an electrical short with the data lines.

6. The display panel as claimed in claim 1, wherein the light leakage prevention film is formed simultaneously

with at least one of the data lines.

7. The display panel as claimed in claim 6, wherein the light leakage prevention film is formed to prevent an electrical short with the gate lines.

8. The display panel as claimed in claim 1, further comprising:

a capacitor metal layer to partially overlap an upper portion of one of the gate lines.

9. A method for manufacturing a display panel including a first substrate having an array region and an array peripheral region, and a second substrate having a black matrix, the method comprising the steps of:

forming a plurality of gate lines on the first substrate;

forming a gate insulating film on the first substrate including the gate lines;

forming a plurality of data lines to cross the gate lines and define a pixel region on the array region; and

forming a light leakage prevention film between the gate lines and/or the data lines of the array peripheral region to prevent light leakage.

10. The display panel according to claim 9, further comprising the steps of:

forming a TFT at a crossing point of a corresponding one of the gate lines and a corresponding one of the data lines;

forming a passivation film on the first substrate including the TFT; and

forming a pixel electrode coupled with the TFT on the passivation film.

11. The method as claimed in claim 10, further

comprising the steps of:

providing the second substrate having the black matrix and a color filter layer; and

forming a liquid crystal layer between the first and second substrates.

12. The method as claimed in claim 9, wherein the light leakage prevention film is formed simultaneously with at least one of the gate lines to prevent light leakage in the display panel.

13. The method as claimed in claim 12, wherein the light leakage prevention film is formed of a conductive material having a high reflectivity.

14. The method as claimed in claim 12, wherein the light leakage prevention film is formed of any one of Cr, Al, Sn, Cu, Mo, Cr/Mo, Cr/Al, or a combination thereof.

15. The method as claimed in claim 12, wherein the light leakage prevention film is formed to prevent an electrical short with the data lines.

16. The method as claimed in claim 9, wherein the light leakage prevention film is formed simultaneously with at least one of the data lines.

17. The method as claimed in claim 16, wherein the light leakage prevention film is formed of a conductive material having a high reflectivity.

18. The method as claimed in claim 16, wherein the light leakage prevention film is are formed of any one of Cr, Al, Sn, Cu, Mo, Cr/Mo, Cr/Al, or a combination thereof.

19. The method as claimed in claim 16, wherein the

light leakage prevention film is formed to prevent an electrical short with the gate lines.

20. The method as claimed in claim 9, further comprising the step of:

forming a capacitor metal layer to partially overlap at least one of the gate lines.

21. The method as claimed in claim 20, wherein the capacitor metal layer is formed simultaneously with at least one of the data lines.